REMARKS

This amendment responds to the Final Office Action mailed June 13, 2006. In the office action the Examiner:

- rejected claims 16-23 and 37-40 under 35 U.S.C. 102(e) as anticipated by Dieffenderfer et al. (US 5,910,930, hereinafter "Dieffenderfer"); and
- objected to claims 24-31 and 41-44 as being dependent upon a rejected base claim.

After entry of this amendment, the pending claims are: claims 16-31 and 37-44.

Assuming that claim 24 is allowed, Applicant requests that the Examiner reinstate withdrawn claims 32-36 and 45-54 based on the allowance of claim 24.

Summary of Interview with the Examiner

During a phone interview on August 1, 2006, the Examiner said that the amendments to claims 24 and 41 would be approved. The Examiner also agreed with the Applicants' arguments that amended claim 16 is not anticipated by Dieffenderfer. The Examiner suggested that claim 37 be amended to clarify that the delay locked loop circuit and the clock receiver circuit are internal to the single chip dynamic random access memory device. The Applicants agreed to consider the Examiner's suggestion and make necessary amendments accordingly. No agreement was reached with respect to the final status of claims 16-23 and 37-40.

Overview of Changes to the Claims

In the Office Action, the Examiner stated that claims 24-31 and 41-44 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Accordingly, to advance the prosecution of the present application towards allowance, the applicants have rewritten claim 24 by including all the limitations of claims 16 and 23 and rewritten claim 41 by including all the limitations of the original claim 37. Therefore, claims 24-31 and 41-44 are in condition for allowance.

Amended claim 16 is directed to a single chip dynamic random access memory device that comprises a core of dynamic random access memory cells, a clock receiver circuit, and a delay locked loop circuit coupled to the clock receiver circuit. Examples of support for the

amendments are found in at least the following portions of the specification of the present application: page 1, lines 16-18, page 4, lines 28-30, page 5, lines 6-7, and page 6, lines 3-4.

Amended claim 37 recites a method of operating a single chip dynamic random access memory device having a core of dynamic random access memory cells, a delay locked loop circuit, and a clock receiver circuit coupled to the delay locked loop circuit. Both the delay locked loop circuit and the clock receiver circuit are turned on in the standby mode. This amendment improves antecedent support for amended claims 38 and 39. Amended claim 39 recites that, during the nap mode, the delay locked loop circuit is in a low power configuration and the clock receiver circuit is on. Examples of support for the amendments to claim 37 are the same as for claim 16, and support for the amendments to claim 39 is found at page 7, lines 11-18 of the specification of the present application.

Claim Rejections - 35 U.S.C. §102(e)

In the Office Action, the Examiner rejected claims 16-23 and 37-40 as being anticipated by Dieffenderfer. The applicants respectfully traverse the rejections.

Claim 16, as amended, is directed to a single chip dynamic random access memory device that includes a core of dynamic random access memory cells, a clock receiver circuit and a delay locked loop circuit coupled to the clock receiver circuit.

Dieffenderfer does not teach or suggest the operation of a single-chip dynamic random access memory device. Dieffenderfer is directed to power management in a microprocessor, and in particular, a clock management scheme that allows the power consumption of the microprocessor to be reduced when normal clocking of some units within the microprocessor is not needed. See, e.g., col. 1, lines 6-17 and Figure 4 of Dieffenderfer.

In claim 16 as amended, the clock receiver circuit and the delay locked loop circuit are internal components of the claimed dynamic random access memory device. For this additional reason, claims 16-23 are not anticipated by Dieffenderfer.

Claim 37, as amended, is directed to a method of operation of a single chip dynamic random access memory device. The memory device has a core of dynamic random access memory cells, a delay locked loop circuit, and a clock receiver circuit coupled to the delay locked loop circuit. The method includes steps of turning off the delay locked loop circuit in a power down mode and turning on the delay locked loop circuit and the clock receiver circuit in a standby power mode.

As noted above, Dieffenderfer does not teach or suggest a single-chip dynamic random access memory device including a delay locked loop circuit and a clock receiver circuit. Nor does Dieffenderfer teach or suggest the steps of operating the delay locked loop circuit and the clock receiver circuit of a single-chip dynamic random access memory device in power down and standby modes in the manner required by claim 37. Therefore claims 37-40 are not anticipated by Dieffenderfer.

CONCLUSION

In light of the above amendments and remarks, the applicants respectfully request that the Examiner reconsider this application with a view towards allowance. The Examiner is invited to call the undersigned attorney if a telephone call could help resolve any remaining items.

Respectfully submitted,

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/ Gary S. Williams / 31,066

Gary S. Williams (Reg. No.)
MORGAN, LEWIS & BOCKIUS LLP
2 Palo Alto Square
3000 El Camino Real, Suite 700
Palo Alto, CA 94306
(650) 843-4000